Multifunctional steep-slope spintronic transistors with spin-gapless-semiconductor or spin-gapped-metal electrodes

Ersoy Şaşıoğlu,* Paul Bodewei, Nicki F. Hinsche, and Ingrid Mertig
Institute of Physics, Martin Luther University Halle-Wittenberg, 06120 Halle (Saale), Germany

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Spin-gapless semiconductors (SGSs) are emerging as a promising class of materials for spintronic applications, offering unique opportunities to realize functionalities beyond conventional electronics. In this work, we propose a concept of multifunctional spintronic field-effect transistors (FETs) using SGSs and/or spin-gapped metals (SGMs) as source and drain electrodes. These devices operate similarly to metal-semiconductor Schottky-barrier FETs, where a potential barrier forms between the SGS (or SGM) electrode and the intrinsic semiconducting channel; however, unlike conventional Schottky-barrier FETs, our proposed devices exploit the distinctive spin-dependent transport properties of SGS and SGM electrodes to achieve sub-60-mV/dec switching, significantly surpassing the 60 mV/dec subthreshold swing (SS) limit in traditional MOSFETs, thereby enabling low-voltage operation. Additionally, the proposed FETs exhibit a nonlocal giant magnetoresistance (GMR) effect, enhancing functionality by enabling nonvolatile memory capabilities. The incorporation of SGMs also introduces a negative differential resistance effect with an ultrahigh peak-to-valley current ratio, further expanding the device's multifunctionality. Two-dimensional (2D) nanomaterials provide a promising platform for realizing these advanced FETs. We perform a comprehensive screening of the computational 2D materials database to identify suitable SGS and SGM candidates. Among the materials identified, several exhibit Curie temperatures significantly above room temperature, ensuring robust ferromagnetic properties for practical applications. For device simulations, we select VS_2 as the SGS material and, as a proof of concept, employ a nonequilibrium Green's function method combined with density functional theory to simulate the transfer (I_D-V_G) and output (I_D-V_D) characteristics of a vertical VS_2/Ga_2O_2 heterojunction FET. Our calculations predict a remarkably low SS of 20 mV/dec, a high on-off ratio of 10^8, and a significant nonlocal GMR effect, demonstrating the potential of these devices for low-power, high-performance logic and memory applications.

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I. INTRODUCTION

Modern charge-based electronics rely heavily on metal-oxide-semiconductor field-effect transistors (MOSFETs) as fundamental building blocks. Their remarkable scaling over the decades has revolutionized computing and communication technologies, enabling the development of increasingly powerful and compact devices; however, despite their widespread use and advancements, conventional MOSFETs face inherent limitations that challenge further progress in electronics scaling and energy efficiency. One such limitation is the 60 mV/dec subthreshold swing (SS) imposed by thermionic emission, which has remained a persistent bottleneck [1,2]. This limitation significantly impedes low-voltage operation, a critical factor for achieving energy-efficient devices in modern electronics. Lowering the operating voltage not only reduces static power consumption but also minimizes leakage currents, addressing a fundamental concern for battery-powered electronics and portable devices, where energy efficiency is paramount. Consequently, the exploration of alternative transistor designs and materials that can overcome these limitations and pave the way for the next generation of energy-efficient electronic devices is of great interest [3–5].

To pass the 60 mV/dec SS limit, alternative transistor designs categorized as steep-slope transistors have been studied with the ultimate goal of achieving a sharper transition between the on and off states, leading to a lower SS value. Examples of such devices include tunnel FETs, Dirac-source FETs, and the recently proposed cold metal source FETs [6–12]. While these alternative designs offer lower SS values compared to conventional MOSFETs,

*Contact author: ersoy.sasioglu@physik.uni-halle.de

they often come with trade-offs. Tunnel FETs, for instance, rely on a tunneling mechanism for current flow, leading to significantly lower on-state currents compared to MOSFETs. This drawback limits their applicability in many logic circuits, where high on-state currents are crucial for driving subsequent stages. In contrast, Dirac-source and cold metal source FETs generally exhibit much higher desired on-state current densities, while by design, their spinless charge transport prohibits the potential benefits offered by the electron's spin additional degree of freedom—a prerequisite for future spintronic devices.

Spin gapless semiconductors (SGSs) have shown promising potential in magnetic tunnel junctions (MTJs), enabling functionalities beyond conventional MTJs based on Fe, Co, and CoFeB. While these traditional MTJs offer high tunnel magnetoresistance (TMR) for memory applications, they lack current rectification, limiting their functionality as diodes for logic applications [13–15]. A recent proposal addressed this by introducing type-II SGSs and half-metallic magnets (HMMs) in MTJs, achieving both TMR and a reprogrammable diode effect [16,17]. The latter concept was experimentally demonstrated in MTJs based on Heusler compounds [18].

Inspired by this progress, we propose a class of spintronic FETs using SGSs and/or spin-gapped metals (SGMs) as source and drain electrodes with an intrinsic semiconducting channel. This configuration overcomes the limitations of both conventional MOSFETs (restricted by the 60 mV/dec SS) and alternative steep-slope transistor designs. The key lies in exploiting the unique spin-dependent transport properties of SGS and SGM electrodes. The SGSs enable sub-60 mV/dec switching and introduce a nonlocal giant magnetoresistance (GMR) effect, which is absent in conventional charge-based FETs. Additionally, SGMs offer negative differential resistance (NDR) with a high peak-to-valley current ratio. These combinations facilitate next-generation applications such as logic-in-memory computing, where data processing and storage occur on the same chip [19–24].

In this paper, we present a comprehensive conceptual framework for multifunctional spintronic FETs. Two-dimensional (2D) nanomaterials emerge as a promising platform for realizing these multifunctional FETs. Their atomically thin structure enables exceptional gate control and mitigates short-channel effects, both of which are essential for low-power, high-performance devices. Focusing on spintronic applications, we identify transition-metal dichalcogenides and dihalides, such as VS_2 and VSi_2N_4, as potential 2D candidates. Through a comprehensive screening of a computational 2D materials database [25], we select suitable SGS and SGM materials for our proposed devices. Notably, many of the identified materials exhibit Curie temperatures well above room temperature, such as VS_2 ($T_C = 437$ K) and VSi_2N_4 ($T_C = 629$ K), ensuring robust ferromagnetic properties for practical applications. To provide a proof of concept, we employ *ab initio* quantum transport calculations to simulate a vertical VS_2/Ga_2O_2 heterojunction FET based on the 2D type-II SGS VS_2. Using a nonequilibrium Green's function method combined with density functional theory, our simulations predict promising device performance, including an SS of only 20 mV/dec, a high on-off ratio of 10^8, and a substantial nonlocal GMR effect. These findings underscore the potential of 2D SGSs for realizing our proposed multifunctional spintronic FETs, paving the way for a new generation of low-power, high-performance spintronic devices.

II. SPIN-GAPLESS SEMICONDUCTORS AND SPIN-GAPPED METALS

The concept of SGSs was introduced by Wang in 2008 [26,27] and subsequently emerged as a promising class of materials for device applications. Using first-principles calculations, Wang predicted SGS behavior in codoped $PbPdO_2$ [26]. Since then, various materials, ranging from two-dimensional to three-dimensional structures, have been theoretically predicted to exhibit SGS behavior [28], with some confirmed experimentally [29]. SGSs occupy a space between magnetic semiconductors and HMMs [30].

Figure 1 depicts a schematic density of states (DOS) for different types of SGSs. In type-I, type-III, and type-IV SGSs, the minority-spin band resembles that of HMMs, but the majority-spin band differs. The valence- and conduction-band edges touch at the Fermi energy, resulting in a zero-gap state. In contrast, type-II SGSs possess a unique band structure in which a finite gap exists just above and below the Fermi level (E_F) for each spin channel; however, the conduction- and valence-band edges of the different spin channels touch. Importantly, SGSs exhibit either ferromagnetic or ferrimagnetic behavior.

One key advantage of type-I, type-III, and type-IV SGSs is that exciting electrons from the valence band to the conduction band requires no energy, and the excited electrons or holes can be 100% spin polarized. Similarly, no energy is needed for spin-flipped Stoner excitations in type-II SGSs. Notably, the mobility of charge carriers in SGSs is generally higher than in conventional semiconductors, making them attractive for nanoelectronic applications. Furthermore, the unique spin-dependent transport properties of SGSs and HMMs hold promise for spintronic devices. Recent proposals include a reconfigurable magnetic tunnel diode and transistor concepts based on these materials [16,18].

We recently introduced a concept in spintronics based on SGMs [31]. This concept builds upon the idea of gapped metals, which are materials possessing a band gap slightly above or below the Fermi level [32–34]. Gapped metals exhibit intrinsic p- or n-type conductivity, unlike

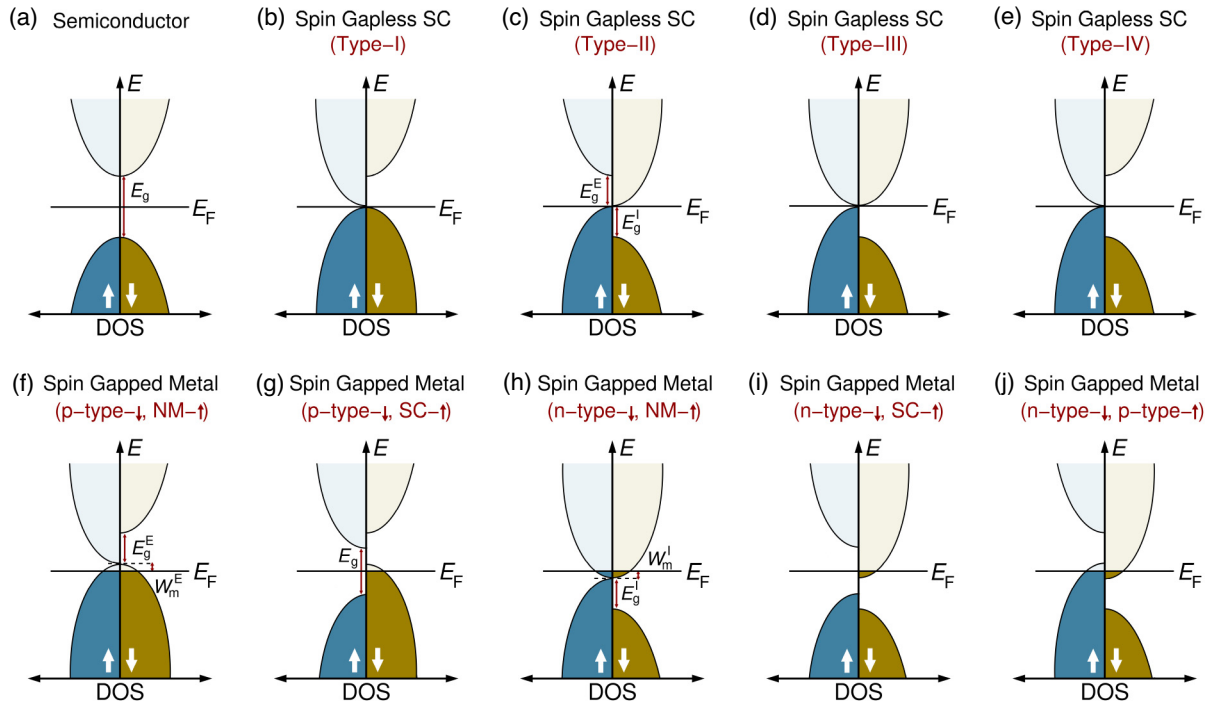

FIG. 1. (a) Schematic representation of the density of states (DOS) of a semiconductor, (b)–(e) spin-gapless semiconductors, and (f)–(j) spin-gapped metals. The arrows represent the two possible spin directions. The horizontal line depicts the Fermi level E_F. Abbreviations: NM, normal metal; SC, semiconductor.

conventional semiconductors, which require extrinsic doping. Similarly, SGMs are predicted to display intrinsic p- or n-type behavior for each spin channel independently. Their properties would be similar to those of dilute magnetic semiconductors, eliminating the requirement for transition-metal doping [35–38]. In Figs. 1(f)–1(j) we present five distinct scenarios of the schematic DOS for spin-gapped metals. By combining p- or n-type gapped metallic behavior for the spin-up electronic band structure with various behaviors such as normal metallic, typical semiconducting, or $n(p)$-type gapped metallic behavior in the spin-down electronic band structure, a broader range of implications for device applications could be achieved, as will be discussed in the next section.

As shown in Fig. 1, SGSs can be qualitatively described by two band-gap parameters: the internal band gap, denoted by E_g^I, and the external band gap, E_g^E. Type-I and type-III SGSs possess an external and an internal band gap, respectively. In contrast, type-II SGSs exhibit both types of band gap. Type-IV SGSs can be regarded as half-metallic magnets. As will be discussed later, these band gaps are crucial in determining the transfer (I_D-V_G) characteristics of SGS-based FETs. SGMs require two additional parameters for the characterization of their electronic structures: W_m^E and W_m^I. Here, W_m^E represents the energy difference between the Fermi level and the valence band maximum (or external band-gap edge) for p-type SGMs, while W_m^I represents the energy difference between the conduction-band minimum (or internal band-gap edge) and the Fermi level for n-type SGMs.

III. MULTIFUNCTIONAL SPINTRONIC FETS

In this section, we introduce a device concept: multifunctional spintronic FETs, as illustrated in Fig. 2. The design leverages SGSs and/or SGMs for the source and drain electrodes, the magnetization direction of which can be configured as either parallel or antiparallel. The channel, in contrast, is formed from an intrinsic semiconductor material. This unique combination creates a structure similar to a Schottky-barrier FET, where a potential barrier

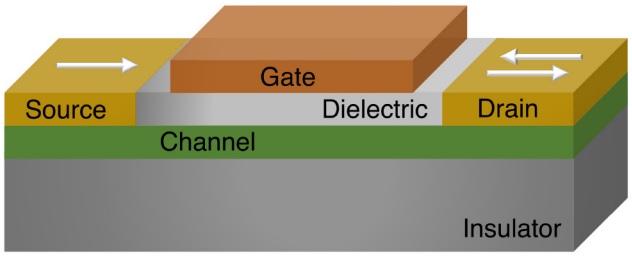

FIG. 2. Schematic representation of a two-dimensional field-effect transistor with spin-gapless semiconductor and/or spin-gapped metal source and drain electrodes. Arrows indicate magnetization direction.

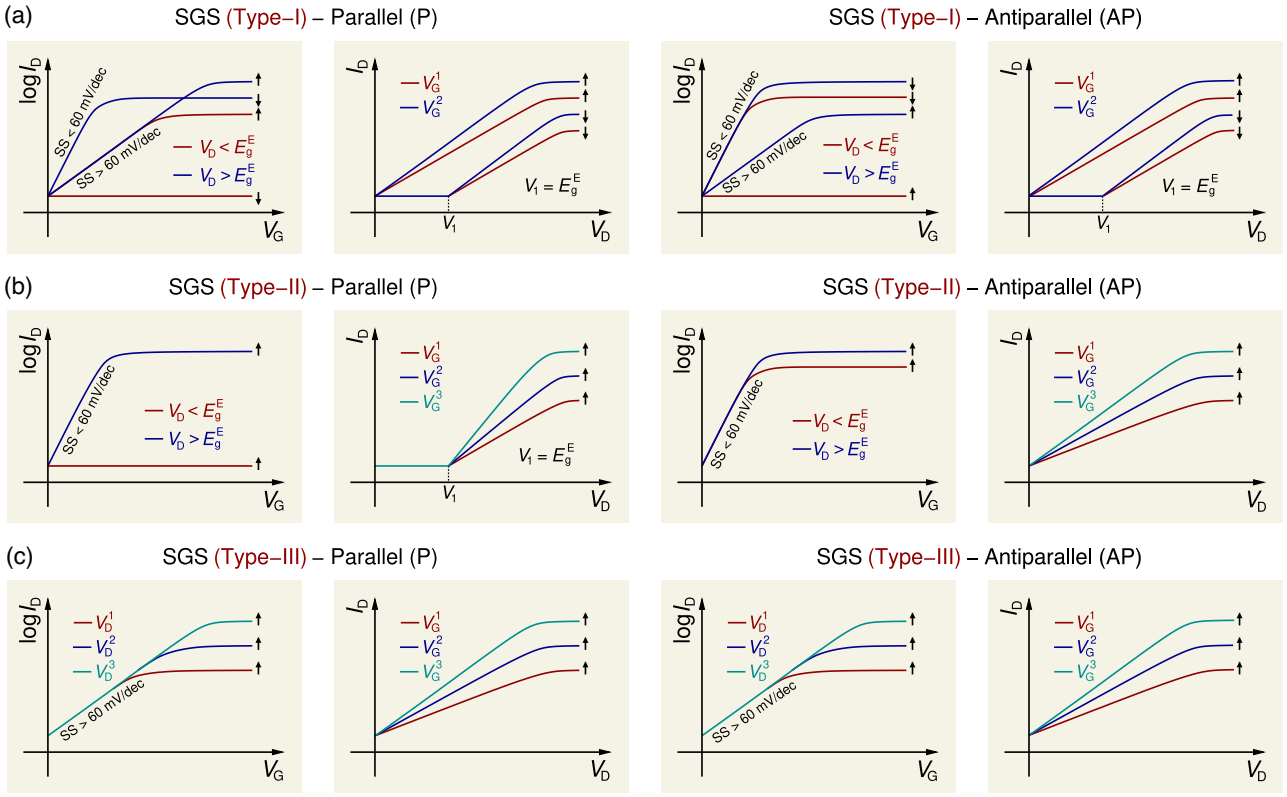

FIG. 3. (a) Schematic representation of the transfer (I_D-V_G) and output (I_D-V_D) characteristics of a FET based on type-I SGS electrodes. The I_D-V_G and I_D-V_D curves are shown for two configurations of the source and drain electrode magnetization directions: parallel and antiparallel. The leftmost panel shows the dependence of drain current (I_D) on gate voltage (V_G) for the majority (spin-up arrow) and minority (spin-down arrow) spin channels at two different drain bias voltages V_D. The adjacent panel illustrates the I_D dependence on drain voltage (V_D) for both spin channels for two different gate voltage V_G. The same configurations are repeated on the right for the antiparallel magnetization case. (b),(c) Similar (I_D-V_G) and output (I_D-V_D) characteristics for FETs based on type-II and type-III SGS electrodes, respectively. Here, SS denotes subthreshold slope.

forms between the SGS (SGM) electrodes and the intrinsic channel. Electron injection in these devices primarily occurs through two mechanisms: (i) thermionic emission, whereby electrons with sufficient thermal energy overcome the Schottky barrier height and are injected into the channel, and (ii) tunneling, whereby a small proportion of electrons can tunnel through the barrier at lower energy levels. The interplay between these mechanisms and the relative alignment of the SGS (SGM) electrode magnetization influences the device's transfer (I_D-V_G) characteristics. By exploring these I_D-V_G characteristics, we aim to understand the potential for manipulating spin currents and achieving functionalities beyond those of conventional FETs.

The schematic transfer (I_D-V_G) and output (I_D-V_D) characteristics for FETs based solely on SGS electrodes are shown in Fig. 3. We consider three types of SGSs (type-I, type-II, and type-III) and explore the influence of the relative magnetization orientation of the source and drain electrodes (parallel and antiparallel) on the drain current. Each SGS type is represented by four panels in Fig. 3, with two panels depicting the drain current (I_D) as a function of gate voltage (V_G) and the other two depicting I_D as a function of drain voltage (V_D). To provide a comprehensive understanding, these panels differentiate between the spin-up and spin-down current components.

Type-I SGSs possess states below the Fermi level in both spin channels, enabling current conduction in both. The first panel of Fig. 3(a) presents the drain current (I_D) versus gate voltage (V_G) for each spin channel with parallel source and drain magnetization. The spin-up channel exhibits conventional FET behavior with an SS exceeding 60 mV/dec; however, the spin-down channel displays different characteristics. For a drain voltage (V_D) lower than the external band gap of the type-I SGS ($V_D < E_g^E$), the drain current (I_D) remains zero. This occurs because the drain electrode lacks unoccupied states to accommodate the incoming electrons from the source. Conversely, when V_D exceeds E_g^E, the spin-down I_D increases exponentially with an SS lower than 60 mV/dec before saturating. This steep-slope behavior originates from the unique spin-dependent band structure of the type-I SGS source

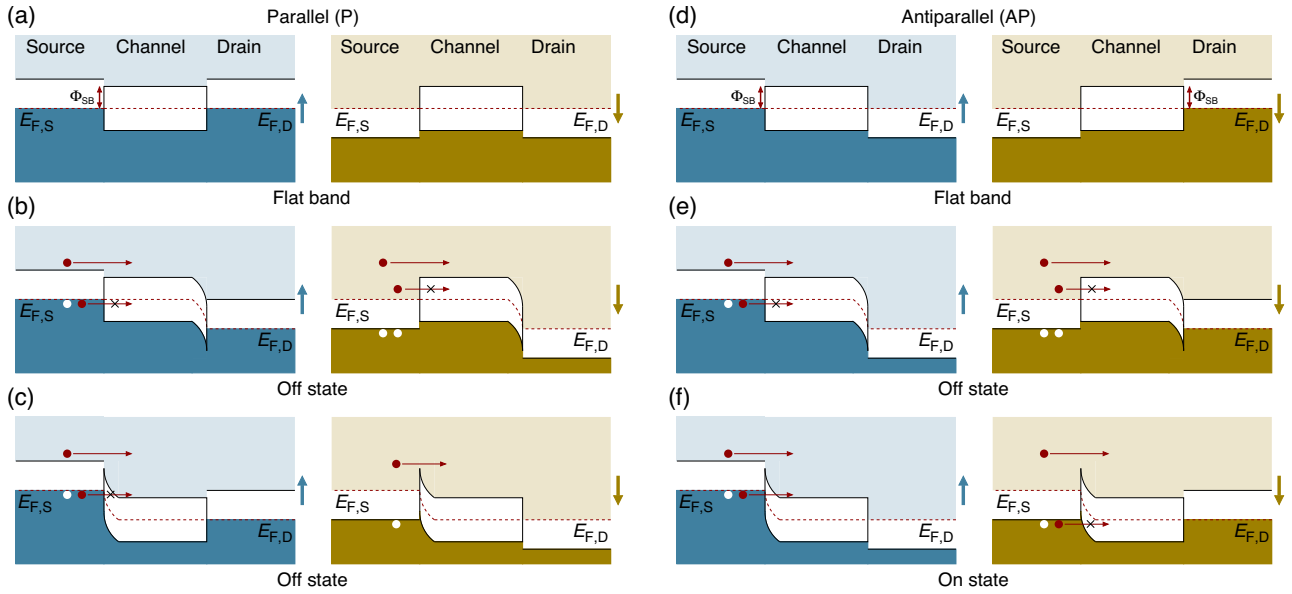

FIG. 4. Schematic illustration of the spin-resolved energy band diagrams of a FET employing type-II SGS electrodes under different magnetization configurations. Panels (a)–(c) correspond to the parallel (P) alignment of the electrode magnetizations, showing (a) the flat-band condition, (b) the off-state, and (c) the on-state. Electrons (holes) are depicted as red (white) spheres, and the Fermi energy is indicated by a dashed line. Panels (d)–(f) show the corresponding diagrams for the antiparallel (AP) magnetization configuration, analogous to (a)–(c).

electrode. High-energy "hot" electrons in the spin-down channel of the source electrode are filtered out, leading to a reduced SS value in the subthreshold region. In the on state, the total I_D is the sum of spin-up and spin-down channel currents. Notably, in the subthreshold region, the overall SS is expected to be lower than 60 mV/dec due to the filtering of high-energy electrons in the spin-down channel. The second panel of Fig. 3(a) shows the output (I_D-V_D) characteristics for fixed gate voltages (V_G^1 and V_G^2) for the spin-up and spin-down channels. For the spin-up channel, I_D increases linearly with V_D. In contrast, the spin-down current remains zero up to a critical drain-source bias voltage V_1 corresponding to the external band gap ($V_1 = E_g^E$). These distinct characteristics highlight the interplay between spin-dependent transport and gate voltage control in type-I SGS FETs. Similar transfer (I_D-V_G) and output (I_D-V_D) characteristics can be observed for the antiparallel magnetization configuration, as shown in the third and fourth panels of Fig. 3(a).

Unlike their type-I counterparts, type-II SGSs possess an internal gap in the opposite spin channel, as illustrated in Fig. 1. Consequently, only the spin-up channel can contribute to the drain current. The resulting I-V characteristics for type-II SGS FETs [Fig. 3(b)] resemble those observed for the spin-down channel in type-I SGS devices. For transistor operation in the parallel magnetization configuration (source and drain magnetizations are aligned), a drain bias voltage exceeding the external band gap (E_g^E) is necessary. Conversely, the antiparallel configuration does not require this condition (see Fig. 4). The external band gap of the type-II SGSs materials considered in this work is larger than 0.5 eV. Therefore, for low-voltage operation, only the antiparallel configuration is applicable. In the parallel configuration, the transistor remains permanently off, leading to a 100% nonlocal GMR effect. In the nonlocal GMR effect, the spin-polarized electrons injected from the SGS source electrode travel ballistically through the channel and are detected by the SGS drain electrode. The resistance of the device varies depending on the relative alignment of the magnetizations of the source and drain: parallel alignment leads to high resistance, while antiparallel alignment results in lower resistance.

In contrast to type-I and type-II SGSs, type-III SGSs exhibit a distinct band structure. They lack a band gap above the Fermi level, leading to conventional transfer characteristics in FETs based on these materials. As shown in Fig. 3, the SS value exceeds 60 mV/dec; however, a band gap exists below the Fermi level in the spin-down channel of these materials, enabling 100% spin-polarized drain current and a nonlocal GMR effect.

The abovementioned nonlocal GMR effect can be defined as $\mathrm{GMR} = \left(I_D^P - I_D^{AP}\right) / \left(I_D^P + I_D^{AP}\right)$, where I_D^P (I_D^{AP}) is the drain current in the parallel (antiparallel) orientation of the magnetization of the source and drain electrodes. While theory predicts a maximum nonlocal GMR of 100% at zero temperature for a FET with ideal SGS electrodes and a channel lacking spin-orbit coupling, real materials exhibit deviations from this ideal SGS behavior. For example, type-II SGS materials have

overlapping valence and conduction bands, resulting in spin-gapped metallic behavior that can reduce the GMR effect. Additionally, finite temperatures introduce thermal excitations (hot electrons) that further diminish the GMR. We will delve deeper into this temperature dependence using the energy-band diagram of a FET based on type-II SGS electrodes.

The energy-band diagrams in Fig. 4 illustrate the operating principles of a FET with type-II SGS source and drain electrodes and an intrinsic semiconductor channel. These diagrams depict the changes in the energy bands for both spin channels under three distinct biasing conditions, considering both parallel and antiparallel magnetization alignments of the source and drain electrodes. In the absence of any applied bias (flat-band condition), the Fermi levels of the SGS electrodes align with the intrinsic level of the semiconductor, resulting in a flat energy-band profile across the device for both spin channels. When a positive bias voltage is applied to the drain electrode relative to the source (off state), the energy bands of the semiconductor bend downward in the vicinity of the drain. In this off state, for sufficiently long channel lengths, minimal current (tunneling leakage current) flows through the device for either spin channel. Finally, applying a positive bias to both the drain and the gate electrode (on state) induces a downward shift in the energy bands of the channel. This allows for spin-up electrons in the source electrode to tunnel through the Schottky barrier and flow into the channel, eventually reaching the drain electrode, turning the FET "on." Note that in Fig. 4, the energy-band diagrams are drawn under the assumption that the drain bias voltage (V_D) is smaller than the external band gap (E_g^E) of the type-II SGS electrodes. This ensures that the transistor is in the off state for parallel electrode magnetization. In this configuration, the absence of unoccupied states in the drain electrode prevents carrier injection. Conversely, for the antiparallel orientation shown in Fig. 4(f), only spin-up electrons can be injected from the source to the drain, resulting in a spin-polarized current.

The steep slope behavior of the FET based on type-II SGSs (see I_D-V_G transfer characteristics in Fig. 3) originates from the presence of a band gap above the Fermi level in the spin-up channel. This energy gap filters out the thermally excited high-energy hot electrons, giving rise to an electron injection within a very narrow energy window at the Fermi level from the source electrode into the drain. The filtering efficiency depends on the magnitude of the external band gap E_g^E. A larger band gap leads to a more efficient filtering effect, blocking higher-energy electrons. The external gaps E_g^E of materials considered in this work range from 0.5 to 0.9 eV. Only a small number of very-high-energy thermally excited electrons, residing at the tail of the Fermi-Dirac distribution can tunnel through the band gap or are thermally injected from either spin channel, as illustrated in the energy-band diagrams of Fig. 4. These "hot electrons" contribute to leakage currents in the off state, diminish the nonlocal GMR effect, and increase the transistor's SS value.

Both type-I and type-II SGS-based transistors exhibit low-voltage operation, achieving SS values below 60 mV/dec provided that the drain voltage is smaller than the external band gap of the SGS electrodes; however, a key difference exists between the two types. Type-I SGS-based FETs function regardless of the relative magnetization direction of the electrodes (as shown in Fig. 3). In contrast, type-II SGS-based FETs only exhibit transistor behavior when the electrodes are in an antiparallel orientation. This limitation in type-II devices is compensated by a significantly stronger nonlocal GMR effect. It is important to note that for type-II SGSs, the spin-gapless semiconducting properties lack inherent symmetry protection and can only emerge when a free parameter, such as pressure, is tuned to a specific value [39]. Consequently, an ideal 2D free-standing type-II SGS material might lose its SGS properties when integrated with a dielectric substrate, as in FETs, or when a heterojunction is formed with other 2D materials. In these scenarios, either an overlap of the spin-up valence and spin-down conduction bands or a shift of the Fermi level into the valence or conduction band occurs, leading to a class of materials we call spin-gapped metals (see Fig. 1). In the following, we discuss the transfer and output characteristics of FETs based on these SGMs.

Our recent paper comprehensively explored the concept of SGMs [31]. While seven distinct types were identified, in this work, we focus on five key cases (illustrated in Fig. 1). We specifically exclude materials in FET design exhibiting p- or n-type spin-gapped behavior in both spin channels. The first considered spin-gapped metal resembles a type-I SGS with a Fermi level shifted into the valence band [Fig. 1(f)]. This configuration leads to metallic behavior in the spin-up channel, while the spin-down channel exhibits p-type characteristics. The transfer (I_D-V_G) characteristics of the corresponding FET presented in Fig. 5(a) resemble those of type-I SGS-based FETs, but with a crucial distinction in the number of distinct drain-source bias voltage regions: unlike type-I SGS FETs (which have two), this device exhibits three. For very small drain biases ($V_D < W_m^E$), both spin channels contribute to the current [Fig. 5(a)]. In the intermediate and high bias region ($W_m^E < V_D < W_m^E + E_g^E$ and $V_D > W_m^E + E_g^E$), the transfer characteristics are similar to type-I SGS FETs. A key advantage of FETs based on p-type spin-gapped metals is the emergence of an NDR effect in the spin-down channel, as shown in the second panel of Fig. 5(a). This behavior contrasts sharply with the linear response observed in SGS-based FETs. For a sufficiently large fixed gate voltage, increasing the drain bias voltage (V_D) in Fig. 5(a) causes the spin-down channel current to initially rise to a peak value. The current then decreases, eventually

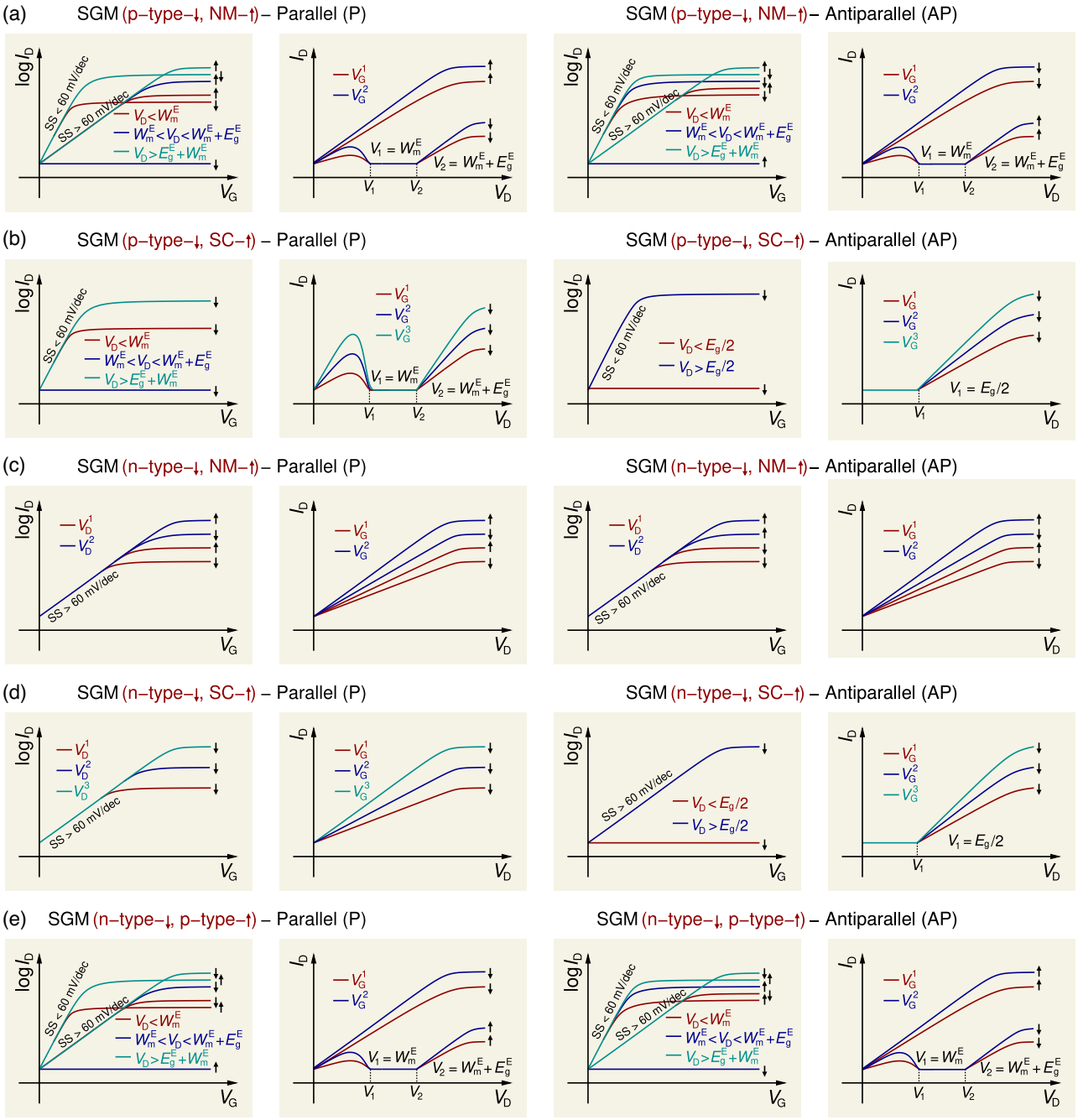

FIG. 5. (a) Schematic representation of the transfer (I_D-V_G) and output (I_D-V_D) characteristics of a FET based on p-type SGM electrodes. The I_D-V_G and I_D-V_D curves depict two configurations of source and drain electrode magnetization directions: parallel and antiparallel. The leftmost panel shows the dependence of the drain current I_D on the gate voltage V_G for the majority (spin-up arrow) and minority (spin-down arrow) spin channels at three different drain bias voltages V_D. The adjacent panel illustrates the I_D dependence on drain voltage (V_D^E) for both spin channels for two different gate voltages V_G. The same configurations are repeated on the right for the antiparallel magnetization case. (b) Transfer (I_D-V_G) and output (I_D-V_D) characteristics of a similar FET with p-type SGM electrodes, but where only the spin-down channel contributes to the drain current. (c),(d) Similar transfer and output characteristics for FETs based on n-type SGMs, following the same panel descriptions as provided for panel (a). (e) Transfer and output characteristics of a FET based on SGM electrodes with a p-type spin-up channel and an n-type spin-down channel. Here, SS denotes subthreshold slope.

reaching zero at $V_D = W_m$ (denoted as V_1 here). Here the current remains zero until another critical voltage, $V_D = W_m + E_g$ (denoted as V_2 here), is reached, after which it increases linearly. In contrast, the spin-up channel current exhibits the typical linear behavior observed in type-I SGS FETs.

The next SGM we consider as an electrode material exhibits a p-type character, but unlike the previous case, one spin channel behaves as a semiconductor instead of a metal. In this FET, only the spin-down channel contributes to the drain current, resulting in transfer (I_D-V_G) and output (I_D-V_D) characteristics [Fig. 5(b)] very similar to those in Fig. 5(a) for the parallel orientation of the electrode magnetization directions; however, for the antiparallel orientation, the semiconducting gap in the spin-up channel of the SGM electrode plays a crucial role in determining the FET's transfer characteristics. At low drain bias voltage ($V_D < E_g/2$), this FET offers a key advantage: a very high nonlocal GMR effect.

In contrast to FETs based on p-type SGMs, those based on n-type SGMs exhibit normal transistor functionality similar to conventional FETs, i.e., with SS values exceeding 60 mV/dec. Figures 5(c) and 5(d) present the corresponding transfer (I_D-V_G) and output (I_D-V_D) characteristics of such FETs based on an n-type SGM with its spin-up channel metallic and its spin-up channel semiconducting, respectively. In the latter case, only the spin-down channel contributes to the drain current, which is therefore spin-polarized. Similar to p-type FETs with one semiconducting spin channel SGM, these n-type FETs also exhibit a very high nonlocal GMR effect.

The final SGM we consider exhibits p-type behavior in the spin-up channel and n-type behavior in the spin-down channel. This p-n-type SGM can be conceptualized as a type-II SGS where the conduction and valence bands overlap. Figure 5(e) shows the transfer and output characteristics of FETs based on these SGMs. As can be seen, the schematic I_D-V_G and I_D-V_D curves are similar to those of FETs based on p-type SGMs with a metallic spin-up channel. Similar to the previous cases, three distinct drain bias voltage regions are observed. For very small drain biases ($V_D < W_m^E$), both spin channels contribute to the current [Fig. 5(e)]. In this regime, the transistor exhibits a gate-tunable NDR effect in the spin-up (spin-down) channel for parallel (antiparallel) alignment of the electrodes' magnetization direction. Notably, the nonlocal GMR effect is observable across all drain bias voltages; it reaches a particularly high value within a specific voltage interval between V_1 and V_2. In this interval, the current in one spin channel diminishes due to the presence of a gap [as seen in the second and fourth panels of Fig. 5(e)]. These FETs based on SGM electrodes exhibit multifunctional characteristics, making them highly attractive for next-generation spintronic devices. Notably, they demonstrate sub-60 mV/dec switching, a hallmark of low-power electronics, alongside the nonlocal GMR effect for efficient spin manipulation and the gate-tunable NDR effect for potential applications in oscillators and high-frequency electronics.

Note that, unlike conventional MOSFETs with bidirectional current flow, the proposed spintronic FETs exhibit a delicate dependence on the source and drain electrode materials. While the focus of this work is on devices with identical SGS or SGM electrodes for both the source and the drain, the spin-dependent nature of these materials offers the potential for exploring current directionality. Using different SGS or SGM materials for the source and drain, as considered in our broader research, could potentially introduce a preference for current flow in one direction. This behavior aligns with our previously proposed reconfigurable magnetic tunnel diode [16,17]; however, a detailed investigation of these mixed-material scenarios would require further study and might be the subject of future research. In the current work, the identical source and drain materials combined with the intrinsic channel create a more MOSFET-like behavior, where the gate voltage primarily controls the overall conductance, enabling bidirectional current flow and on-off switching functionality.

Having established the potential of FETs based on SGS and SGM electrodes through analysis of their schematic transfer and output characteristics, we now want to specifically validate these promising results through detailed quantum transport calculations based on first principles for specific devices. The following sections detail the chosen computational approach, the screening process for identifying promising 2D SGS and SGM materials, and finally, quantum transport calculations performed on a vertical FET employing a selected SGS material.

IV. COMPUTATIONAL METHOD

We employed density functional theory (DFT), as implemented in the QUANTUMATK package [40,41], to calculate the ground-state electronic structure of the materials. For the exchange-correlation functional, the generalized gradient approximation (GGA) within the Perdew-Burke-Ernzerhof (PBE) parametrization [42] was used in conjunction with PSEUDO DOJO pseudo potentials [43] and linear combination of atomic orbitals (LCAO) basis sets. A dense k-point grid of $24 \times 24 \times 1$ and a density mesh cutoff of 120 Ha were employed. To eliminate interactions between periodic images, a vacuum layer of 20 Å was added, and Neumann boundary conditions were applied. The convergence criteria for total energy and forces were set to at least 10^{-4} eV and 0.01 eV/Å, respectively.

The GGA-PBE exchange-correlation functional [42] was chosen for its demonstrated accuracy in capturing key electronic properties relevant to device simulations, such as valence band maximum, conduction band minimum, and band widths. This choice is supported by previous studies on isoelectronic materials such as NbS_2, $NbSe_2$, and TaS_2 (known as cold metals), where extensive GW calculations revealed minimal deviations in these critical features compared to the PBE results, despite significant differences in internal band gaps [44]. Furthermore,

TABLE I. Summary of key properties for the studied compounds: lattice constants (a and b), sublattice and total magnetic moments (m_{TM} and m_{total}), magnetic anisotropy energy (MAE), work function (Φ), spin-gap type per spin direction, internal and external energy gaps ($E_g^{I/E}$), formation energy (E_{form}), convex hull distance (ΔE_{con}), and mean-field Curie temperature. Data for a, b, MAE, E_{form}, and ΔE_{con} are sourced from the Computational 2D Materials Database (C2DB) [25]. The corresponding crystal structures are shown in the Supplemental Material in Fig. S1.

Compound	a (Å)	b (Å)	m_{TM} (μ_B)	m_{total} (μ_B)	MAE (meV)	Φ (eV)	SGS type	$E_g^{I/E}$ (eV)	E_{form} (eV/at.)	E_{con} (eV/at.)	T_c^{MFA} (K)
$Ti_4Cl_4Te_4$	7.07	7.07	1.13	4.00	1.47 (y)	4.60	Type-I	/0.59	−1.03	0.096	248
V_3MoSe_8	6.67	5.77	1.04 (1.12)	3.00	2.42 (y)	5.33	Type-I	/0.72	−0.68	0.026	207
VSi_2N_4	2.88	2.88	1.17	1.00	0.10 (y)	5.60	Type-II	1.73/0.58	−0.95		629
VS_2	3.18	3.18	1.08	1.00	0.21 (y)	5.76	Type-II	0.78/0.75	−0.88	0.000	437
VSSe	3.26	3.26	1.18	1.00	0.40 (y)	5.29	Type-II	0.56/0.50	−0.79	0.010	439
ScI_2	3.98	3.98	0.92	1.00	0.51 (y)	3.47	Type-II	2.47/0.82	−1.14	0.008	206

previous investigations on 2D materials, including VSe_2, have shown that PBE provides reliable semiquantitative predictions for structural and electronic properties, with only minor changes observed in GW calculations [25]. These findings underscore the suitability of PBE for the qualitative and semiquantitative analysis presented in this work.

Transport calculations were performed using a combination of DFT and the nonequilibrium Green's function (NEGF) method implemented within QUANTUMATK. A dense k-point grid of $24 \times 1 \times 172$ was employed for self-consistent DFT-NEGF calculations. The transfer and output characteristics were obtained using the Landauer approach [45], where the current is expressed as $I(V) = 2e/h \sum_\sigma \int T^\sigma(E,V)\,[f_L(E,V) - f_R(E,V)]\,\mathrm{d}E$. In this equation, V represents the applied bias voltage, $T^\sigma(E,V)$ is the spin-dependent transmission coefficient for an electron with spin σ, and $f_L(E,V)$ and $f_R(E,V)$ are the Fermi-Dirac distribution functions for the left and right electrodes, respectively. The transmission coefficient, $T^\sigma(E,V)$, is calculated using a finer k-point grid of 300×1.

V. RESULTS AND DISCUSSION

The preceding section of this manuscript established the concept of multifunctional spintronic FETs through a conceptual foundation. We explored the transfer and output characteristics of these devices based on the schematic spin-resolved DOS and energy-band diagrams for SGSs and SGMs used as electrode materials. This section builds upon that foundation by presenting the results of our computational investigations and some discussion of them. We will detail the screening process employed to identify promising 2D SGS and SGM candidates using DFT calculations. Following this, we will showcase the design and exploration of a specific vertical heterojunction FET example using VS_2 (a type-II SGS) as the source and drain electrodes.

A. Screening of 2D SGSs and SGMs

Three-dimensional (3D) SGSs have been extensively studied, both experimentally and theoretically [29,39,46–49]; however, for next-generation low-power and miniaturized electronics, 2D materials offer significant advantages due to their unique properties and potential for device scaling [50–53]. A crucial advantage of 2D materials in this context is the ability to tune the Schottky barrier height at the interface between the channel material and the electrodes using a gate voltage [54–59]. This gate control over the barrier allows for more flexible device operation compared to their 3D counterparts. Identifying suitable 2D SGSs and SGMs is crucial for realizing the multifunctional spintronic FETs proposed in this work. Ideal candidates should possess specific properties to achieve the desired functionalities. We conducted a search in the C2DB [25,60] and identified 6 SGSs and 11 SGMs, as outlined in Tables I and II, respectively. Our initial criterion for selecting materials for the study was their formation energy, E_{form}, which we required to be negative; however, negative E_{form} alone does not guarantee stability. The convex hull distance E_{con}, which represents the energy difference between the studied structure and the most stable phase or a mixture of phases, is also crucial. Typically, values less than 0.1 eV/atom are desired to facilitate the growth of a material [61]. All materials selected from the C2DB for our study exhibit E_{con} values less than the cutoff of 0.1 eV/atom.

While negative formation energy and low convex hull distance are crucial indicators of material stability and growth, the Curie temperature (T_C) is another key factor for the practical use of SGSs and SGMs as source and drain electrodes. For device applications, it is essential for SGSs and SGMs to exhibit ferromagnetism at or above room temperature. We performed systematic calculations of the Heisenberg exchange parameters to estimate T_C values within the mean-field approximation. These values, presented in Tables I and II, serve as upper limits, with rigorous methods such as the random phase approximation

TABLE II. Summary of key properties for the studied compounds: lattice constants (a and b), sublattice and total magnetic moments (m_{TM} and m_{total}), magnetic anisotropy energy (MAE), work function Φ, spin-gap type per spin direction, the distance of the Fermi level from the edge of the band that it crosses $W_{\mathrm{m}}^{\mathrm{I,E}(\uparrow/\downarrow)}$ (see text for more details), energy gap per spin direction $E_{\mathrm{g}}^{\mathrm{I,E}(\uparrow/\downarrow)}$, formation energy ($E_{\mathrm{form}}$), convex hull distance energy (ΔE_{con}), and mean-field Curie temperature. Data for a, b, MAE, E_{form}, and ΔE_{con} are sourced from the Computational 2D Materials Database [25,60]. The corresponding crystal structures are shown in the Supplemental Material in Fig. S2.

Compound	a (Å)	b (Å)	m_{TM} (μ_B)	m_{total} (μ_B)	MAE (meV)	Φ (eV)	Spin-gap type	$W_{\mathrm{m}}^{\mathrm{I,E}(\uparrow/\downarrow)}$ (eV)	$E_{\mathrm{g}}^{\mathrm{I,E}(\uparrow/\downarrow)}$ (eV)	E_{form} (eV/at.)	E_{con} (eV/at.)	$T_{\mathrm{C}}^{\mathrm{MFA}}$ (K)
V_3MoS_8	6.37	5.51	0.49 (0.57)	1.46	−0.10 (z)	5.80	p-type-↑/p-type-↓	0.34/0.75	0.85/0.94	−0.87	0.020	206
$VOsO_2Br_4$	5.24	5.24	1.49 (0.47)	1.99	3.70 (y)	5.28	p-type-↑/p-type-↓	0.21/0.47	0.59/0.88	−0.96	0.036	65
$Cr_2Br_2Te_2$	5.46	3.76	3.54	6.10	−2.95 (z)	5.59	NM-↑/p-type-↓	/0.38	/0.85	−0.51	0.000	446
$Cr_2I_2Te_2$	5.43	3.93	3.55	6.05	−3.13 (z)	5.03	NM-↑/p-type-↓	/0.16	/0.94	−0.35	0.000	436
$Cr_3Cl_2O_4$	5.42	5.42	2.83 (2.99)	8.00	−0.46 (z)	5.84	p-type-↑ /SC-↓	0.15/	0.89/	−1.61	0.090	731
$PdCr_2Se_4$	3.69	3.69	3.27	5.43	0.29 (x)	5.44	p-type-↑/p-type-↓	0.61/0.51	0.37/0.66	−0.42	0.080	534
Cr_3S_4	3.44	3.44	3.06 (−3.22)	2.51	0.03 (x)	5.20	n-type-↑/n-type-↓	0.37/0.34	0.29/0.43	−0.66	0.050	632
$Cr_4F_2N_3$	3.01	3.01	3.00 (−2.82)	0.42	−0.08 (z)	5.11	NM-↑/n-type-↓	/0.18	/0.74	−1.09	0.030	1045
$CrGa_2S_4$	3.72	3.72	3.79	3.60	-0.05 (z)	3.71	n-type-↑/n-type-↓	0.27/0.48	1.12/1.68	-0.64	0.050	347
$CrGa_2Se_4$	3.92	3.92	3.95	3.80	−0.19 (z)	3.93	n-type-↑/n-type-↓	0.50/0.65	0.71/0.92	−0.55	0.060	564
$CoGa_2S_4$	3.61	3.61	0.91	1.00	0.07 (x)	4.19	n-type-↑ /SC-↓	0.35/	0.56/	−0.57	0.050	309

method or Monte Carlo simulations required for more accurate predictions. Among the studied materials, several exhibit promising T_{C} values significantly above room temperature. For instance, VS_2, used as a source and drain electrode in our proposed FET design, demonstrates a mean-field T_{C} of 437 K, making it highly suitable for practical applications. VSi_2N_4, a type-II SGS, shows an even higher T_{C} of 629 K, indicating robust ferromagnetic properties. Cr_3S_4 and $Cr_4F_2N_3$ also exhibit exceptional T_{C} values of 632 K and 1045 K, respectively, further highlighting the potential of these materials for high-temperature spintronic applications. In addition, $PdCr_2Se_4$ and $CrGa_2Se_4$ show T_{C} values of 534 and 564 K, respectively, which are well above room temperature. These materials, with their high T_{C} values, stable structures, and favorable magnetic properties, stand out as strong candidates for practical device applications. Furthermore, 2H-VSe_2, known for its above-room-temperature ferromagnetism [62,63], demonstrates the potential for heterostructures to enhance material properties. When combined with other 2D materials such as MoS_2 or WS_2, charge-transfer effects in VSe_2 could transform it into an SGM while maintaining a T_{C} value above room temperature.

The electronic and magnetic properties of the identified SGS materials in Table I are particularly attractive for FET applications. Of key importance are the internal and, especially, the external band gaps ($E_{\mathrm{g}}^{\mathrm{I/E}}$). A large external band gap is crucial for filtering out high-energy hot electrons in FETs, enabling sub-60-mV/dec SS values, as discussed in the preceding section. As shown in Table I, all considered compounds possess calculated external band gaps exceeding 0.5 eV. Furthermore, the V-based compounds exhibit lattice parameters compatible with existing 2D semiconductors, such as MoS_2, MoSSe, $MoSi_2N_4$, and others [64,65]. This compatibility facilitates seamless integration of these V-based SGS materials with established 2D semiconductors within FET devices. It is important to note that while type-IV SGS behavior exists in some 2D materials [66], these materials are excluded from our analysis due to their lack of relevance for steep-slope FET applications.

Similar to the SGS materials discussed previously, the electronic properties of the SGMs presented in Table II are crucial for FET applications. As with SGS materials, a large external band gap, exceeding 0.5 eV, is desired for efficient hot-electron filtering and achieving sub-60-mV/dec SS values. All materials listed in Table II fulfill this criterion; however, for SGMs, an additional parameter, $W_{\mathrm{m}}^{\mathrm{I,E}(\uparrow/\downarrow)}$, comes into play. This parameter represents the energy difference between the valence (conduction) band edge and the Fermi level for p-type (n-type) SGMs, but crucially, it is specific to each spin direction (represented by the arrows). Table II reveals that some SGMs exhibit either p- or n-type character for both spin channels, while others exhibit mixed behavior, with one spin channel being semiconducting or metallic and the other exhibiting p- or n-type character. For the p-type SGMs, the calculated $W_{\mathrm{m}}^{\mathrm{E}(\uparrow/\downarrow)}$ values range from 0.16 to 0.75 eV, with similar values observed for n-type SGMs. As discussed earlier for p-type SGM-based FETs, the $W_{\mathrm{m}}^{\mathrm{E}(\uparrow/\downarrow)}$ parameter significantly impacts the NDR characteristics and the valley bias voltage in the I_{D}-V_{D} curves. While a larger $W_{\mathrm{m}}^{\mathrm{I,E}(\uparrow/\downarrow)}$ value leads to a higher valley bias voltage, it also comes at the cost of higher SS values, as reported for gapped metals (or cold metals) in FETs [12]. Therefore, achieving an optimal balance between $W_{\mathrm{m}}^{\mathrm{E}(\uparrow/\downarrow)}$ and the external band gap, $E_{\mathrm{g}}^{\mathrm{E}(\uparrow/\downarrow)}$, is crucial for tailoring the transfer and output characteristics of FETs based on p-type SGMs.

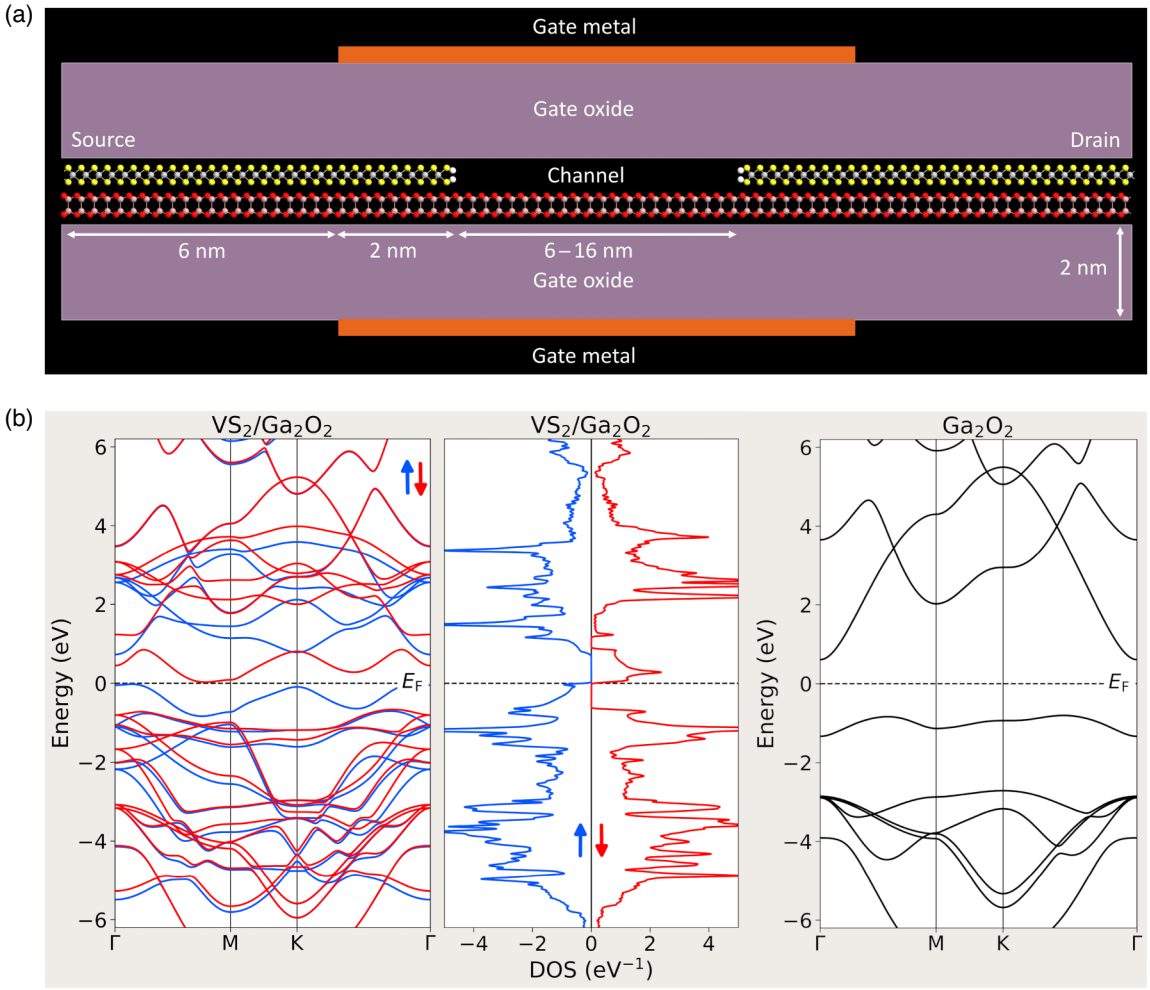

FIG. 6. (a) Schematic of a vertical VS_2/Ga_2O_2 heterojunction FET with key dimensions labeled. Channel length varies from 6 to 16 nm, while the thicknesses of the source and drain, gate overlap lengths, and gate oxide are fixed at 6, 2, and 2 nm, respectively. (b) Calculated spin-resolved band structure along the high-symmetry directions and corresponding density of states (DOS) for the VS_2/Ga_2O_2 source and drain (left panels) and the band structure of Ga_2O_2 channel material (right panel). The dashed black line indicates the Fermi level set to zero energy.

The computational screening process successfully identified a range of promising 2D SGS and SGM candidates for multifunctional spintronic FETs. These materials exhibit a compelling combination of electronic and magnetic properties, including large external band gaps for efficient hot-electron filtering. The V-based SGS materials stand out due to their lattice parameters, which seamlessly integrate with existing 2D semiconductors, paving the way for straightforward device fabrication.

B. Vertical VS_2/Ga_2O_2 heterojunction FET

Following the identification of promising 2D material candidates, this subsection explores a specific vertical heterojunction FET design using VS_2 (a type-II SGS) as the source and drain electrodes and Ga_2O_2 as the channel material. This configuration leverages VS_2's properties to achieve the functionalities outlined earlier. Ga_2O_2 is chosen for the channel due to its small electron effective mass ($0.33m_0$), lattice matching, and comparable work function to VS_2. We first discuss the device geometry and then the electronic structure of the source, drain, and channel materials. The chosen device geometry adopts a vertical configuration with dual gates, as illustrated in Fig. 6. The source and drain electrodes (fixed at 6 nm) are composed of a VS_2/Ga_2O_2 heterostructure. The channel length varies from 6 to 16 nm, and the gate electrode overlaps the source and drain by 2 nm with a 2-nm-thick gate oxide (dielectric constant of 25). It is worth noting that the channel material, Ga_2O_2, has a slightly smaller lattice constant (3.13 Å) than VS_2 (3.18 Å). To achieve a lattice-matched interface, the Ga_2O_2 experiences a slight tensile in-plane strain during heterostructure formation.

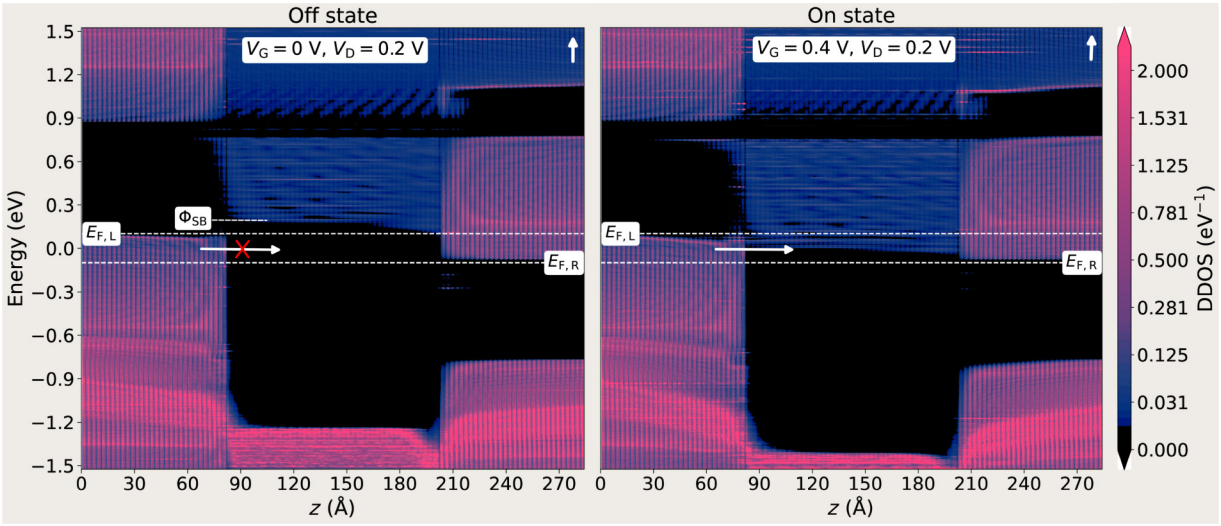

FIG. 7. Projected device density of states (DDOS) for majority spin (spin-up) electrons in a 12-nm channel length vertical VS_2/Ga_2O_2 heterostructure FET [see Fig. 6(a) for device structure]. Left panel: off state. Right panel: on state. Upper and lower white dashed lines indicate the Fermi levels of the source and drain electrodes, respectively, and Φ_{SB} denotes the Schottky barrier.

Varying the channel length from 6 to 16 nm allows us to investigate its impact on subthreshold swing and leakage current. Due to the coherent transport mechanism, the on-state current is expected to be less dependent on channel length within this range. Shorter channels, however, can suffer from increased off-state currents due to enhanced leakage currents through the channel. By exploring this range of channel lengths, we aim to identify an optimal balance between achieving a low SS value (indicating sharp switching) and minimizing leakage current for efficient device operation.

We opted for a VS_2/Ga_2O_2 heterostructure for the source and drain electrodes instead of a pure VS_2 monolayer. This choice maintains the type-II SGS character crucial for device applications, as evident from the spin-resolved band structure of the heterostructure in Fig. 6(b) and projected bands presented in the Supplemental Material [67]. Additionally, it simplifies the device design, reducing computational costs during simulations. As shown in Fig. 6(b), the vertical VS_2/Ga_2O_2 heterostructure exhibits ideal type-II SGS behavior, with occupied spin-up and unoccupied spin-down bands aligned at the Fermi level. The channel material, Ga_2O_2, possesses a suitable band gap of 1.56 eV and a favorable electron effective mass of $0.33m_0$; however, the hole effective mass is significantly heavier, at $3.13m_0$. The calculated work function for the Ga_2O_2 channel ($\Phi = 6.36$ eV) is higher than that of the source and drain electrodes ($\Phi = 5.81$ eV). This difference creates a Schottky barrier of 0.17 eV at both the source-channel and channel-drain interfaces.

In the Supplemental Material (Fig. S4), we present the spin-resolved local device density of states (DDOS) for a vertical VS_2/Ga_2O_2 heterostructure FET under antiparallel electrode magnetization and flat-band conditions (zero gates and drain bias). The 12-nm-channel DDOS clearly illustrates Schottky barriers at both the source-channel and channel-drain interfaces. Figure 7 depicts the spin-up channel DDOS for the off-state ($V_G = 0$ V, $V_D = 0.2$ V) and on-state ($V_G = 0.4$ V, $V_D = 0.2$ V) conditions, as the spin-up channel is the only current carrier in type-II SGS materials. For completeness, the DDOS for the spin-down channel is presented in the Supplemental Material [67]. As seen in Fig. 7, the off-state DDOS indicates a drain-bias-induced barrier reduction near the channel-drain interface. In contrast, the on state exhibits a gate-voltage-tuned Schottky barrier, decreasing from 0.17 to 0 eV. This reduction facilitates efficient electron injection from the source into the channel, contributing to a substantial drain current. It is worth noting that experimental observations of similar gate-voltage-induced Schottky-barrier modulation have been reported in 2D-material-based FETs [54–59].

The transfer characteristics (I_D-V_G) of the vertical VS_2/Ga_2O_2 heterostructure FET were calculated under the antiparallel electrode magnetization configuration for three different source-drain bias voltages (0.1, 0.2, and 0.3 V). As discussed in Sec. III, in contrast to the parallel configuration, this configuration enables low-voltage transistor operation. The channel length was varied from 6 to 16 nm in 2-nm increments. Figure 8 presents representative I_D-V_G curves for channel lengths of 8, 12, and 16 nm. The transistor exhibits a sharp transition from the off state to the on state within a narrow gate voltage range of 0.2–0.4 V. For gate voltages exceeding 0.5 V, the on-state current saturates at 100 μA/μm. While the saturated currents for drain voltages of 0.2 and 0.3 V are comparable, the off-state currents differ by more than an order of magnitude, and this is attributable to drain-induced barrier

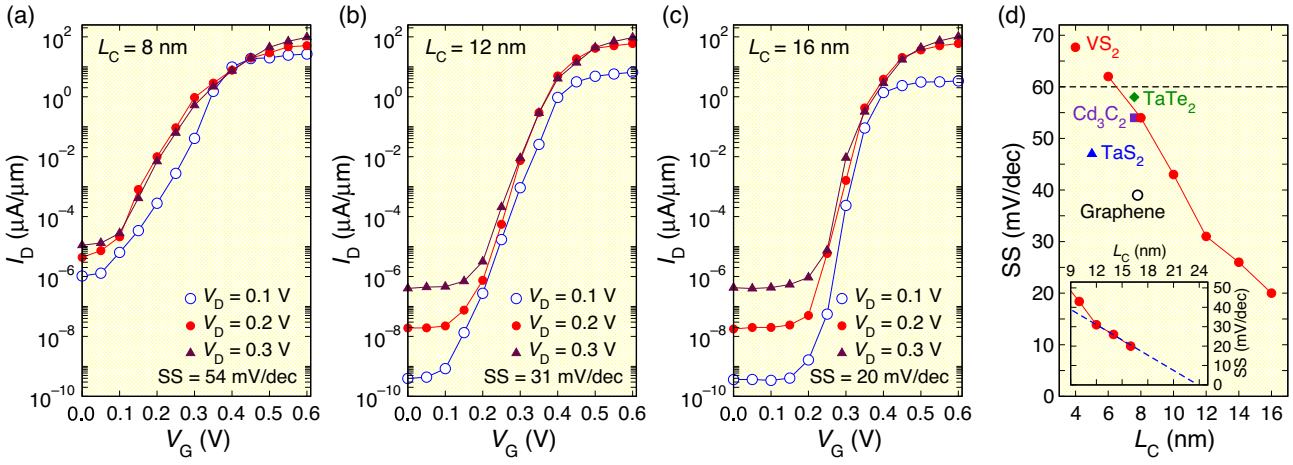

FIG. 8. Calculated transfer characteristics (I_D-V_G) of the vertical VS_2/Ga_2O_2 heterostructure FET for three different source-drain bias voltages. The calculations were performed assuming antiparallel magnetization orientations of the source and drain electrodes. (a)–(c) Curves of I_D-V_G for channel lengths (L_C) of 8, 12, and 16 nm, respectively. (d) Subthreshold slope (SS) as a function of channel length. The dashed line represents the thermionic limit. The SS values for cold-source FETs such as TaS_2 are taken from Ref. [10]. Inset: extrapolation of SS to longer channel lengths.

lowering. Figure 8(d) shows the SS values as a function of channel length (L_C), with SS values of cold-source 2D material FETs included for comparison. The obtained SS value for a 6-nm channel slightly surpasses the room-temperature thermionic limit of 60 mV/dec; however, the SS decreases almost linearly with increasing channel length, reaching 20 mV/dec at 16 nm. The inset of Fig. 8(d) shows an extrapolation of the SS to longer channel lengths, indicating the potential for ideal transistor behavior (SS = 0 mV/dec) at around 24 nm. It is worth noting that threshold switch FETs based on 2D materials have reported an exceptionally low SS of 0.33 mV/dec [68].

The on-state current density of the SGS FET is a key performance metric. For all investigated channel lengths, this value consistently reaches approximately 100 μA/μm when applying drain-source bias voltages of 0.2 and 0.3 V. Notably, this value drops by an order of magnitude at 0.1 V, likely due to wave-function mismatching between the source and drain electrodes. This observed current density significantly surpasses the much lower on-state values reported for tunnel FETs [10], highlighting the potential advantages of our SGS FET architecture in terms of driving-current capability. Furthermore, the device exhibits an on-off ratio exceeding 10^8 for channel lengths greater than 10 nm, demonstrating its excellent switching behavior. These combined characteristics position the SGS FET as a promising candidate for high-performance, low-power electronic applications, particularly where high current drive and steep subthreshold slope are essential.

SGSs can be regarded as the theoretical ultimate limit of cold metals for steep-slope FETs [69–71]. As previously discussed, cold-source and cold-metal FETs hold promise for surpassing the conventional thermionic limit of 60 mV/dec for the SS value at room temperature; however, reported SS values for cold-metal FETs remain relatively high [8,10]. This limitation arises from the electronic band structure of the cold-metal electrodes. The energy-gap edge (W_m^E) above the Fermi level [see Figs. 1(f) and 1(g)] and the external band gap (E_g^E) play a crucial role in filtering high-energy electrons. In cold metals with large W_m^E values, only electrons in the deep subthreshold regime are effectively filtered, not those in the crucial subthreshold region. The cold metal $NbTe_2$-based FET exemplifies this behavior [8]. Its intrinsic W_m^E of 0.5 eV can be reduced to 0.27 eV by applying a 9% strain, leading to an improved SS of 23 mV/dec in a $NbTe_2$-based FET. Type-I and type-II SGSs offer the potential to overcome this limitation by possessing an energy-gap edge (W_m^E) approaching zero. Theoretically, this would enable ideal switching behavior with an SS of 0 mV/dec in an SGS-based FET under coherent transport conditions. Nevertheless, inelastic scattering processes, such as electron-phonon interactions, can still degrade the SS value in cold-metal FETs, as has been demonstrated theoretically [72,73].

Given the potential of SGS materials for ideal switching, we examined the performance of vertical VS_2/Ga_2O_2 heterostructures FET under antiparallel and parallel electrode magnetization configurations. As previously discussed, the antiparallel magnetization configuration of the type-II SGS source and drain electrodes is crucial for low-voltage, energy-efficient transistor operation. In contrast, the parallel magnetization configuration results in an off state for drain-source voltages below the drain electrode's external spin gap (E_g^E) of approximately 0.8 eV. Figure 9(a) illustrates this behavior, showing a sharp increase in drain current (I_D) only after the drain-source bias voltage (V_D) exceeds 0.8 V. This phenomenon is attributed to the

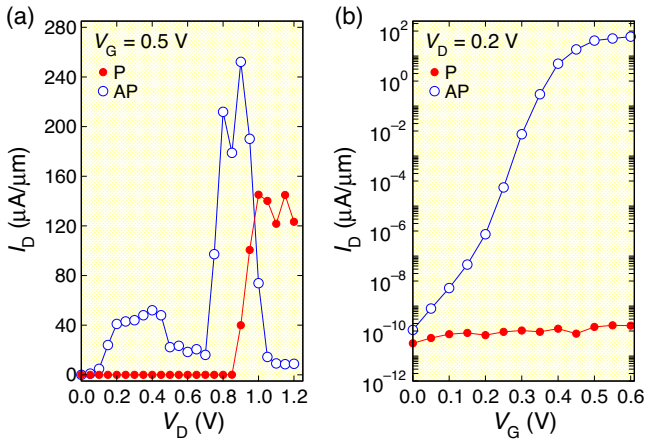

FIG. 9. (a) Output characteristics (I_D-V_D) of a 12-nm channel length vertical VS_2/Ga_2O_2 heterojunction FET. Drain current (I_D) is plotted as a function of source-drain bias voltage (V_D) for a fixed gate voltage of 0.5 V, comparing parallel (P) and antiparallel (AP) magnetization configurations of the source and drain electrodes at 300 K. (b) Transfer characteristics (I_D-V_G) of the same device at 0 K. Drain current (I_D) is plotted as a function of gate voltage (V_G) for a fixed source-drain voltage of 0.2 V, comparing P and AP magnetization configurations.

electronic structure of the source and drain electrodes [Fig. 6(b)] and the coherent transport mechanism, which prevents spin-up electrons from reaching the drain due to the spin gap. For $V_D = 1$ V and a gate voltage of 0.5 V, I_D surpasses 140 μV/μm. Conversely, the antiparallel magnetization configuration leads to a nonmonotonic I_D-V_D relationship due to the electrode's 2D electronic structure. For example, I_D nearly vanishes at $V_D = 1.1$ V due to a gap in unoccupied spin-down states [Fig. 6(b)]. Overall, our calculated transfer and output characteristics align well with the device concept presented earlier.

The distinct behavior of our vertical VS_2/Ga_2O_2 heterostructure FET under parallel and antiparallel electrode magnetization configurations manifests as a pronounced nonlocal GMR effect. As shown in Fig. 9(b), the drain current (I_D) is entirely suppressed for the parallel configuration due to the unique band structure of the type-II SGS electrodes, which prohibits current flow. In contrast, the antiparallel configuration enables typical transistor operation with I_D exponentially increasing with gate voltage, resulting in a 100% nonlocal GMR effect at 0 K. It is important to note that the current version of the QUANTUMATK package does not incorporate the necessary treatment of temperature effects via Fermi-Dirac distribution for SGS materials, as discussed in Ref. [74]. Consequently, the transfer (I_D-V_G) characteristics presented in Fig. 9(b) are limited to 0 K. Conversely, for the antiparallel magnetization configuration, temperature effects are considered, and the corresponding transfer characteristics are shown in Fig. 8 at 300 K.

To fully explore the potential of SGS materials for FET applications, a comprehensive investigation encompassing a wider range of compounds is necessary. While this study focuses on the vertical VS_2-based FET as a proof of concept, the promising results motivate further exploration of the materials listed in Table I. Type-II SGS materials, such as VSSe, are anticipated to exhibit similar device characteristics, while type-I SGS compounds such as $Ti_4Cl_4Te_4$ may offer comparable functionalities with potentially larger SS values due to electron transport in both spin channels (see Fig. 1). These materials warrant in-depth theoretical and experimental investigations to assess their suitability for high-performance FETs. To further enhance FET performance, we turn our attention to SGMs. Unlike SGSs, SGMs offer a broader range of functionalities when integrated as source and drain electrodes in FETs, as previously detailed in Sec. III. Essentially, SGMs can be considered as cold metals with an additional degree of freedom: spin polarization. This enables not only the conventional steep-slope transistor operation and gate-tunable NDR effect associated with cold metals but also introduces the nonlocal GMR effect. A critical parameter influencing the SS value of cold-metal-based FETs is the energy-gap edge (W_m^E) above the Fermi level [Figs. 1(f) and 1(g)]. Traditional 2D cold metals exhibit relatively large W_m^E values, typically between 0.5 and 1 eV, which can hinder device performance [71,75]. In contrast, the SGMs presented in Table II offer significantly smaller W_m^E values, ranging from 0.11 to 0.75 eV, potentially leading to improved FET characteristics.

Future research should focus on heterostructures comprising different material combinations to fully realize the potential of SGS and SGM materials for FET applications. While this study focused on devices with identical source and drain electrodes, enabling conventional MOSFET-like operation, the integration of distinct SGS or SGM materials offers exciting possibilities. For instance, a FET incorporating a type-II SGS source electrode and a type-IV SGS drain electrode could function as a reconfigurable dynamical diode, allowing current flow in a specific direction determined by electrode magnetization. This concept, previously proposed by the present authors and experimentally demonstrated, holds significant promise for extended device functionalities [16,18]. By systematically investigating various material combinations, it is anticipated that a rich landscape of device behaviors can be explored, leading to the development of innovative electronic and spintronic devices.

Finally, it is essential to acknowledge the limitations of the present study in the context of practical device implementation. While our theoretical investigations highlight the promising potential of SGS- and SGM-based FETs, several aspects warrant further exploration. The Curie temperatures (T_C) of the studied materials, estimated using the mean-field approximation, should be considered

as upper limits. More rigorous methods, such as classical Monte Carlo simulations, which include the effects of magnetic anisotropy energy, are required to obtain more accurate T_C values. This is particularly important for 2D magnets, as the Mermin-Wagner theorem suggests that long-range magnetic order is suppressed in the absence of sufficient anisotropy. Furthermore, a detailed understanding of the temperature-dependent electronic and magnetic properties of SGSs and SGMs is crucial for accurate device modeling and optimization. In this study, the temperature dependence of these characteristics was assumed to be negligible; however, future investigations must address this aspect to ensure realistic predictions for device operation.

VI. SUMMARY AND CONCLUSIONS

In this paper, we propose a concept for multifunctional spintronic FETs leveraging SGSs and SGMs as source and drain electrodes. Our findings highlight the substantial advantages of these materials in overcoming the subthreshold-swing limitations of conventional MOSFETs, achieving SS values well below the 60 mV/dec threshold. This advancement facilitates low-voltage operation, positioning these devices as promising candidates for energy-efficient electronic applications. Furthermore, the observed nonlocal GMR effect and NDR effect, characterized by ultrahigh peak-to-valley current ratios, underscore the multifunctionality of these FETs, enabling the seamless integration of logic and memory functionalities within a single device. Through a systematic screening of the Computational 2D Materials Database, we identified several SGS and SGM materials suitable for spintronic applications. Using VS_2 as the SGS material, our device simulations of a vertical VS_2/Ga_2O_2 heterostructure FET demonstrate the feasibility of achieving exceptionally low SS values of 20 mV/dec, high on-off ratios of 10^8, and pronounced nonlocal GMR effects. These results illustrate the potential of 2D materials for enabling advanced multifunctional spintronic devices.

The integration of spintronic functionalities into FETs opens exciting opportunities for next-generation electronics by combining ultralow power consumption with high computational speed and memory density; however, several challenges remain before the potential of SGS and SGM materials can be fully exploited in practical applications. While this study provides a strong foundation, further efforts are required to identify materials with optimal properties, such as robust ferromagnetic ordering at higher temperatures. The mean-field Curie temperatures (T_C) reported here represent upper limits; more rigorous techniques, such as Monte Carlo simulations including magnetic anisotropy energy, are necessary to obtain accurate predictions for 2D magnets. Additionally, a deeper understanding of the temperature-dependent electronic and magnetic characteristics of SGSs and SGMs is critical for realistic device modeling and optimization. Future research should focus on improving the scalability, reliability, and compatibility of these devices with existing semiconductor technologies. The ability to precisely engineer and control spin-dependent transport at the nanoscale will be pivotal to the success of multifunctional spintronic FETs. This progress could pave the way for novel computing architectures, such as logic-in-memory devices, that leverage both the charge and spin degrees of freedom.

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DATA AVAILABILITY

The data that support the findings of this article are not publicly available. The data are available from the authors upon reasonable request.

[1] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices* (Cambridge University Press, Cambridge, 2021).
[2] M. Lundstrom, Fundamentals of carrier transport, 2nd edn, Meas. Sci. Technol. **13**, 230 (2002).
[3] H.-S. P. Wong and S. Salahuddin, Memory leads the way to better computing, Nat. Nanotechnol. **10**, 191 (2015).
[4] A. M. Ionescu and H. Riel, Tunnel field-effect transistors as energy-efficient electronic switches, Nature **479**, 329 (2011).
[5] I. Ferain, C. A. Colinge, and J.-P. Colinge, Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors, Nature **479**, 310 (2011).
[6] A. M. Ionescu, in *Nanoelectronics: Materials, Devices, Applications*, edited by K. Iniewski (Wiley-VCH, Weinheim, 2017), pp. 137–152.
[7] C. Qiu, F. Liu, L. Xu, B. Deng, M. Xiao, J. Si, L. Lin, Z. Zhang, J. Wang, and H. Guo *et al.*, Dirac-source field-effect transistors as energy-efficient, high-performance electronic switches, Science **361**, 387 (2018).
[8] F. Liu, Switching at less than 60 mV/decade with a "cold" metal as the injection source, Phys. Rev. Appl. **13**, 064037 (2020).
[9] Z. Tang, C. Liu, X. Huang, S. Zeng, L. Liu, J. Li, Y.-G. Jiang, D. W. Zhang, and P. Zhou, A steep-slope MoS_2/graphene Dirac-source field-effect transistor with a large drive current, Nano Lett. **21**, 1758 (2021).
[10] S. Wang, J. Wang, T. Zhi, J. Xue, D. Chen, L. Wang, and R. Zhang, Cold source field-effect transistors: Breaking the 60-mV/decade switching limit at room temperature, Phys. Rep. **1013**, 1 (2023).
[11] S. Wang, X. Liu, and P. Zhou, The road for 2D semiconductors in the silicon age, Adv. Mater. **34**, 2106886 (2022).

[12] Y. Yin, Z. Zhang, C. Shao, J. Robertson, and Y. Guo, Computational study of transition metal dichalcogenide cold source MOSFETs with sub-60 mV per decade and negative differential resistance effect, Npj 2D Materials and Applications **6**, 55 (2022).

[13] J. Mathon and A. Umerski, Theory of tunneling magnetoresistance of an epitaxial Fe/MgO/Fe (001) junction, Phys. Rev. B **63**, 220403 (2001).

[14] S. S. Parkin, C. Kaiser, A. Panchula, P. M. Rice, B. Hughes, M. Samant, and S.-H. Yang, Giant tunnelling magnetoresistance at room temperature with MgO (100) tunnel barriers, Nat. Mater. **3**, 862 (2004).

[15] C. Chappert, A. Fert, and F. N. Van Dau, The emergence of spin electronics in data storage, Nat. Mater. **6**, 813 (2007).

[16] E. Şaşıoğlu, S. Blügel, and I. Mertig, Proposal for reconfigurable magnetic tunnel diode and transistor, ACS Appl. Electron. Mater. **1**, 1552 (2019).

[17] T. Aull, E. Şaşıoğlu, N. Hinsche, and I. Mertig, *Ab initio* study of magnetic tunnel junctions based on half-metallic and spin-gapless semiconducting Heusler compounds: Reconfigurable diode and inverse tunnel-magnetoresistance effect, Phys. Rev. Appl. **18**, 034024 (2022).

[18] N. Maji and T. K. Nath, Demonstration of reconfigurable magnetic tunnel diode and giant tunnel magnetoresistance in magnetic tunnel junctions made with spin gapless semiconductor and half-metallic Heusler alloy, Appl. Phys. Lett. **120**, 072401 (2022).

[19] E. Linn, R. Rosezin, S. Tappertzhofen, U. Böttger, and R. Waser, Beyond von Neumann–logic operations in passive crossbar arrays alongside memory operations, Nanotechnology **23**, 305205 (2012).

[20] T. You, Y. Shuai, W. Luo, N. Du, D. Bürger, I. Skorupa, R. Hübner, S. Henker, C. Mayr, and R. Schüffny *et al.*, Exploiting memristive $BiFeO_3$ bilayer structures for compact sequential logics, Adv. Funct. Mater. **24**, 3357 (2014).

[21] S. Gao, F. Zeng, M. Wang, G. Wang, C. Song, and F. Pan, Implementation of complete boolean logic functions in single complementary resistive switch, Sci. Rep. **5**, 15467 (2015).

[22] Y. Zhou, Y. Li, L. Xu, S. Zhong, H. Sun, and X. Miao, 16 Boolean logics in three steps with two anti-serially connected memristors, Appl. Phys. Lett. **106**, 233502 (2015).

[23] Z.-R. Wang, Y.-T. Su, Y. Li, Y.-X. Zhou, T.-J. Chu, K.-C. Chang, T.-C. Chang, T.-M. Tsai, S. M. Sze, and X.-S. Miao, Functionally complete boolean logic in 1T1R resistive random access memory, IEEE Electron Device Lett. **38**, 179 (2017).

[24] K. M. Kim, N. Xu, X. Shao, K. J. Yoon, H. J. Kim, R. S. Williams, and C. S. Hwang, Single-cell stateful logic using a dual-bit memristor, Phys. Status Solidi Rapid Res. Lett. **13**, 1800629 (2019).

[25] S. Haastrup, M. Strange, M. Pandey, T. Deilmann, P. S. Schmidt, N. F. Hinsche, M. N. Gjerding, D. Torelli, P. M. Larsen, and A. C. Riis-Jensen *et al.*, The computational 2D materials database: High-throughput modeling and discovery of atomically thin crystals, 2D Materials **5**, 042002 (2018).

[26] X. L. Wang, Proposal for a new class of materials: Spin gapless semiconductors, Phys. Rev. Lett. **100**, 156404 (2008).

[27] X. Wang, G. Peleckis, C. Zhang, H. Kimura, and S. Dou, Colossal electroresistance and giant magnetoresistance in doped $PbPdO_2$ thin films, Adv. Mater. **21**, 2196 (2009).

[28] X. Wang, Z. Cheng, G. Zhang, H. Yuan, H. Chen, and X.-L. Wang, Spin-gapless semiconductors for future spintronics and electronics, Phys. Rep. **888**, 1 (2020).

[29] S. Ouardi, G. H. Fecher, C. Felser, and J. Kübler, Realization of spin gapless semiconductors: The Heusler compound Mn_2CoAl, Phys. Rev. Lett. **110**, 100401 (2013).

[30] R. A. de Groot, F. M. Mueller, P. G. v. van Engen, and K. H. J. Buschow, New class of materials: Half-metallic ferromagnets, Phys. Rev. Lett. **50**, 2024 (1983).

[31] E. Şaşıoğlu, M. Tas, S. Ghosh, W. Beida, B. Sanyal, S. Blügel, I. Mertig, and I. Galanakis, Spin gapped metals: A novel class of materials for multifunctional spintronic devices, J. Magn. Magn. Mater. **615**, 172792 (2025).

[32] O. I. Malyi and A. Zunger, False metals, real insulators, and degenerate gapped metals, Appl. Phys. Rev. **7**, 041310 (2020).

[33] F. Ricci, A. Dunn, A. Jain, G.-M. Rignanese, and G. Hautier, Gapped metals as thermoelectric materials revealed by high-throughput screening, J. Mater. Chem. A **8**, 17579 (2020).

[34] M. R. Khan, H. R. Gopidi, and O. I. Malyia, Optical properties and electronic structures of intrinsic gapped metals: Inverse materials design principles for transparent conductors, Appl. Phys. Lett. **123**, 061101 (2023).

[35] K. Sato, L. Bergqvist, J. Kudrnovský, P. H. Dederichs, O. Eriksson, I. Turek, B. Sanyal, G. Bouzerar, H. Katayama-Yoshida, V. A. Dinh, T. Fukushima, H. Kizaki, and R. Zeller, First-principles theory of dilute magnetic semiconductors, Rev. Mod. Phys. **82**, 1633 (2010).

[36] B.-H. Lei and D. J. Singh, Computational search for itinerant *n*-type and *p*-type magnetic semiconductors: Arsenopyrites as bipolar magnetic semiconductors, Phys. Rev. B **105**, L121201 (2022).

[37] N. T. Tu, P. N. Hai, L. D. Anh, and M. Tanaka, (Ga,Fe)Sb: A *p*-type ferromagnetic semiconductor, Appl. Phys. Lett. **105**, 132402 (2014).

[38] K. Kroth, B. Balke, G. H. Fecher, V. Ksenofontov, C. Felser, and H.-J. Lin, Diluted magnetic semiconductors with high Curie temperature based on C1(b) compounds: $CoTi_{1-x}Fe_xSb$, Appl. Phys. Lett. **89**, 202509 (2006).

[39] T. Aull, E. Şaşıoğlu, I. V. Maznichenko, S. Ostanin, A. Ernst, I. Mertig, and I. Galanakis, *Ab initio* design of quaternary Heusler compounds for reconfigurable magnetic tunnel diodes and transistors, Phys. Rev. Mater. **3**, 124415 (2019).

[40] S. Smidstrup, D. Stradi, J. Wellendorff, P. A. Khomyakov, U. G. Vej-Hansen, M.-E. Lee, T. Ghosh, E. Jónsson, H. Jónsson, and K. Stokbro, First-principles Green's-function method for surface calculations: A pseudopotential localized basis set approach, Phys. Rev. B **96**, 195309 (2017).

[41] S. Smidstrup *et al.*, QuantumATK: an integrated platform of electronic and atomic-scale modelling tools, J. Phys. Condens. Matter **32**, 015901 (2019).

[42] J. P. Perdew, K. Burke, and M. Ernzerhof, Generalized gradient approximation made simple, Phys. Rev. Lett. **77**, 3865 (1996).

[43] M. J. Van Setten, M. Giantomassi, E. Bousquet, M. J. Verstraete, D. R. Hamann, X. Gonze, and G.-M. Rignanese,

The PseudoDojo: Training and grading a 85 element optimized norm-conserving pseudopotential table, Comput. Phys. Commun. **226**, 39 (2018).

[44] W. Beida, E. Şaşıoğlu, M. Tas, C. Friedrich, S. Blügel, I. Mertig, and I. Galanakis, Correlation effects in two-dimensional MX_2 and MA_2Z_4 (M = Nb, Ta; X = S, Se, Te; A = Si, Ge; Z = N, P) cold metals: Implications for device applications, Phys. Rev. Mater. **9**, 014006 (2025).

[45] M. Büttiker, Y. Imry, R. Landauer, and S. Pinhas, Generalized many-channel conductance formula with application to small rings, Phys. Rev. B **31**, 6207 (1985).

[46] K. Özdoğan, E. Şaşıoğlu, and I. Galanakis, Slater-Pauling behavior in LiMgPdSn-type multifunctional quaternary Heusler materials: Half-metallicity, spin-gapless and magnetic semiconductors, J. Appl. Phys. **113**, 193903 (2013).

[47] I. Galanakis, K. Özdoğan, and E. Şaşıoğlu, Spin-filter and spin-gapless semiconductors: The case of Heusler compounds, AIP Adv. **6**, 055606 (2016).

[48] G. Z. Xu, E. K. Liu, Y. Du, G. J. Li, G. D. Liu, W. H. Wang, and G. H. Wu, A new spin gapless semiconductors family: Quaternary Heusler compounds, EPL **102**, 17007 (2013).

[49] Q. Gao, I. Opahle, and H. Zhang, High-throughput screening for spin-gapless semiconductors in quaternary Heusler compounds, Phys. Rev. Mater. **3**, 024410 (2019).

[50] A. K. Geim and K. S. Novoselov, The rise of graphene, Nat. Mater. **6**, 183 (2007).

[51] M. Chhowalla, D. Jena, and H. Zhang, Two-dimensional semiconductors for transistors, Nat. Rev. Mater. **1**, 1 (2016).

[52] A. Allain, J. Kang, K. Banerjee, and A. Kis, Electrical contacts to two-dimensional semiconductors, Nat. Mater. **14**, 1195 (2015).

[53] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, and M. S. Strano, Electronics and optoelectronics of two-dimensional transition metal dichalcogenides, Nat. Nanotechnol. **7**, 699 (2012).

[54] H. Yang, J. Heo, S. Park, H. J. Song, D. H. Seo, K.-E. Byun, P. Kim, I. Yoo, H.-J. Chung, and K. Kim, Graphene barristor, a triode device with a gate-controlled Schottky barrier, Science **336**, 1140 (2012).

[55] W. J. Yu, Z. Li, H. Zhou, Y. Chen, Y. Wang, Y. Huang, and X. Duan, Vertically stacked multi-heterostructures of layered materials for logic transistors and complementary inverters, Nat. Mater. **12**, 246 (2013).

[56] R. Moriya, T. Yamaguchi, Y. Inoue, S. Morikawa, Y. Sata, S. Masubuchi, and T. Machida, Large current modulation in exfoliated-graphene/MoS_2/metal vertical heterostructures, Appl.Phys. Lett. **105**, 083119 (2014).

[57] D. Qiu and E. K. Kim, Electrically tunable and negative Schottky barriers in multi-layered graphene/MoS_2 heterostructured transistors, Sci. Rep. **5**, 13743 (2015).

[58] A. Dankert and S. P. Dash, Electrical gate control of spin current in van der Waals heterostructures at room temperature, Nat. Commun. **8**, 16093 (2017).

[59] S. W. LaGasse, P. Dhakras, K. Watanabe, T. Taniguchi, and J. U. Lee, Gate-tunable graphene–WSe_2 heterojunctions at the Schottky–Mott limit, Adv. Mater. **31**, 1901392 (2019).

[60] M. N. Gjerding, A. Taghizadeh, A. Rasmussen, S. Ali, F. Bertoldo, T. Deilmann, N. R. Knøsgaard, M. Kruse, A. H. Larsen, and S. Manti *et al.*, Recent progress of the computational 2D materials database (C2DB), 2D Materials **8**, 044002 (2021).

[61] A. Novick, D. Cai, Q. Nguyen, R. Garnett, R. Adams, and E. Toberer, Probabilistic prediction of material stability: Integrating convex hulls into active learning, Mater. Horiz. **11**, 5381 (2024).

[62] X. Wang, D. Li, Z. Li, C. Wu, C.-M. Che, G. Chen, and X. Cui, Ferromagnetism in 2D vanadium diselenide, ACS Nano **15**, 16236 (2021).

[63] P. Jiang, L. Kang, H. Hao, X. Zheng, Z. Zeng, and S. Sanvito, Ferroelectric control of electron half-metallicity in a-type antiferromagnets and its application to nonvolatile memory devices, Phys. Rev. B **102**, 245417 (2020).

[64] Y.-L. Hong, Z. Liu, L. Wang, T. Zhou, W. Ma, C. Xu, S. Feng, L. Chen, M.-L. Chen, and D.-M. Sun *et al.*, Chemical vapor deposition of layered two-dimensional $MoSi_2N_4$ materials, Science **369**, 670 (2020).

[65] B. Mortazavi, B. Javvaji, F. Shojaei, T. Rabczuk, A. V. Shapeev, and X. Zhuang, Exceptional piezoelectricity, high thermal conductivity and stiffness and promising photocatalysis in two-dimensional $MoSi_2N_4$ family confirmed by first-principles, Nano Energy **82**, 105716 (2021).

[66] Q. Sun and N. Kioussis, Prediction of manganese trihalides as two-dimensional Dirac half-metals, Phys. Rev. B **97**, 094408 (2018).

[67] See Supplemental Material at http://link.aps.org/supplemental/10.1103/PhysRevApplied.23.044022 for further insights into the characteristics of the devices.

[68] J. Hu, H. Li, A. Chen, Y. Zhang, H. Wang, Y. Fu, X. Zhou, K. P. Loh, Y. Kang, J. Chai, C. Wang, J. Zhou, J. Miao, Y. Zhao, S. Zhong, R. Zhao, K. Liu, Y. Xu, and B. Yu, All-2D-materials subthreshold-free field-effect transistor with near-ideal switching slope, ACS Nano **18**, 20236 (2024).

[69] L. Zhang and F. Liu, High-throughput approach to explore cold metals for electronic and thermoelectric devices, Npj Comput. Mater. **10**, 78 (2024).

[70] D. Logoteta, J. Cao, M. Pala, P. Dollfus, Y. Lee, and G. Iannaccone, Cold-source paradigm for steep-slope transistors based on van der Waals heterojunctions, Phys. Rev. Res. **2**, 043286 (2020).

[71] L. Wang, Y. Shi, M. Liu, A. Zhang, Y.-L. Hong, R. Li, Q. Gao, M. Chen, W. Ren, and H.-M. Cheng *et al.*, Intercalated architecture of MA_2Z_4 family layered van der Waals materials with emerging topological, magnetic and superconducting properties, Nat. Commun. **12**, 2361 (2021).

[72] R. Duflou, M. Houssa, and A. Afzalian, in *2021 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)* (IEEE, Dallas, Texas, 2021), p. 94.

[73] A. Afzalian, Ab initio perspective of ultra-scaled CMOS from 2D-material fundamentals to dynamically doped transistors, Npj 2D Materials and Applications **5**, 5 (2021).

[74] E. Şaşıoğlu, T. Aull, D. Kutschabsky, S. Blügel, and I. Mertig, Half-metal–spin-gapless-semiconductor junctions as a route to the ideal diode, Phys. Rev. Appl. **14**, 014082 (2020).

[75] E. Şaşıoğlu and I. Mertig, Theoretical prediction of semiconductor-free negative differential resistance tunnel diodes with high peak-to-valley current ratios based on two-dimensional cold metals, ACS Appl. Nano Mater. **6**, 3758 (2023).